What is claimed is:

1. An automatic adjusting method, wherein a phase shift amount CLK_DLY has a maximum value DLY_MAX, and a phase shift amount DLY_MAX+1 corresponds to a full-cycle shift of phase, said method comprising:

a first step of waiting for an interrupt of a vertical synchronization signal which serves as a trigger pulse, and transitioning to a next step when the interrupt is generated;

a second step of setting the phase shift amount CLK_DLY to zero, and supplying phase control data (CLK_DLY=0) to a phase controller by a CPU;

a third step of waiting for an interrupt of the vertical synchronization signal which serves as a trigger pulse, and transitioning to a fourth step when the interrupt is generated, wherein a video detector calculates data from one screen of video at CLK_DLY for use in an automatic adjustment, and transfers video detection data (VIDEO_DATA(CLK_DLY)) at CLK_DLY to a video detection data memory when the interrupt is generated;

a fourth step of confirming whether the phase shift amount CLK_DLY has reached the maximum value DLY_MAX, transitioning to a seventh step when the phase shift amount has reached the maximum value, and transitioning to a fifth step when the phase shift amount has not reached the maximum value;

a fifth step of incrementing the phase shift amount CLK_DLY by one and setting the incremented phase shift amount, and supplying the phase control data (CLK_DLY=CLK_DLY+1) from said

CPU to said phase controller;

a sixth step of reading video detection data (VIDEO_DATA(CLK_DLY−1)) from said video detection data memory by said CPU, holding the read video detection data in a RAM of said CPU as optimal phase determination data at each phase set value, and returning again to said third step when a processing at this sixth step is completed;

processings from said third step to said sixth step being repeated until a condition at said fourth step is satisfied;

a seventh step of reading video detection data (VIDEO_DATA(DLY_MAX)) when CLK_DLY=DLY_MAX from said video detection data memory by said CPU, said CPU acquiring optimal phase determination data at each of phase set values CLK_DLY=0 to DLY_MAX;

an eighth step of analyzing, by said CPU, the optimal phase determination data at each of the phase set values to calculate an optimal phase value; and

a ninth step of supplying the calculated optimal phase value from said CPU to said phase controller as phase control data, wherein said phase controller controls a phase delay amount for a clock pulse in accordance with the phase control data, supplies the phase-controlled clock pulse to an A/D converter as a sampling pulse, such that said A/D converter samples an analog video input signal at an optimal phase to convert the analog video input signal to a digital video signal, said digital video signal being supplied to a digital video signal processor, said digital video signal processor performing a color correction and a scaling processing on the digital video signal to convert the digital video signal to

a digital video signal for display on a display unit, said display unit displaying the digital video signal as a video.

2. An automatic adjusting circuit comprising:

an A/D converter for sampling an analog video input signal with a sampling pulse to convert the analog video input signal to a digital video signal;

a digital video signal processor for performing a color correction and a scaling processing on the digital video signal;

a display unit for displaying the signal processed digital video signal;

a clock pulse generator for generating a clock pulse from a horizontal synchronization signal, said analog video input signal being sampled with said clock pulse;

a phase controller for controlling a phase of said clock pulse;

a CPU for supplying frequency control data and phase control data for said clock pulse, and for controlling respective peripheral circuits;

a phase control data memory for holding the phase control data from said CPU, said phase control data memory being triggered by a vertical synchronization signal to transfer the phase control data to said phase controller;

a video detector for calculating video detection data for use in an automatic adjustment from the digital video signal, said video detector being triggered by the vertical synchronization signal to supply the video detection data; and

a video detection data memory for holding the video detection data, and supplying the video detection data in response to a reading operation of said CPU.

3. An automatic adjusting method, wherein a phase shift amount CLK_DLY has a maximum value DLY_MAX, and a phase shift amount DLY_MAX+1 corresponds to a full-cycle shift of phase, said method comprising:

a first step of setting the phase shift amount CLK_DLY to zero, and supplying phase control data (CLK_DLY=0) to a phase control data memory by a CPU;

a second step of waiting for an interrupt of a vertical synchronization signal which serves as a trigger pulse, and transferring phase control data (CLK_DLY=0) from said phase control data memory to a phase controller when the interrupt is generated;

a third step of setting the phase-shift amount CLK_DLY to one, and supplying phase control data (CLK_DLY=1) to said phase control data memory by said CPU;

a fourth step of waiting for an interrupt of the vertical synchronization signal which serves as a trigger pulse, and transferring phase control data (CLK_DLY) from said phase control data memory to said phase controller when the interrupt is generated, wherein a video detector calculates data for use in an automatic adjustment from one screen of video at CLK_DLY − 1, and transfers video detection data (VIDEO_DATA(CLK_DLY − 1)) to a video detection data memory when the interrupt is generated;

a fifth step of confirming whether the phase shift amount CLK_DLY has reached the maximum value DLY_MAX, transitioning to an eighth step when the phase shift amount has reached the maximum value, and transitioning to a sixth step when the phase shift amount has not reached the maximum value;

a sixth step of incrementing the phase shift amount CLK_DLY by one and setting the incremented phase shift amount, and supplying the phase control data (CLK_DLY=CLK_DLY+1) to said phase control data memory by said CPU;

a seventh step of reading video detection data (VIDEO_DATA(CLK+DLY−2)) from said video detection data memory, holding the read video detection data in a RAM of said CPU as optimal phase determination data at each phase set value, returning again to said fourth step when a processing at this seventh step is completed;

processings from said fourth step to said seventh step being repeated until a condition at said fifth step is satisfied;

an eighth step of reading video detection data (VIDEO_DATA(DLY_MAX−1)) when CLK_DLY=DLY_MAX−1 from said video detection data memory by said CPU;

a ninth step of waiting for an interrupt of the vertical synchronization signal which serves as a trigger pulse, wherein said video detector calculates data for use in automatic adjustment from one screen of video at CLK_DLY=DLY_MAX, and transfers video detection data (VIDEO_DATA(DLY_MAX) when CLK_DLY=DLY_MAX to said video detection data memory when the interrupt is generated;

a tenth step of reading video detection data

(VIDEO_DATA(DLY_MAX) when CLK_DLY=DLY_MAX from said video detection data memory by said CPU, said CPU acquiring optimal phase determination data at each of phase set values CLK_DLY=0 to DLY_MAX;

an eleventh step of analyzing by said CPU the acquired optimal phase determination data at each of the phase set values to calculate an optimal phase value; and

a twelfth step of supplying the calculated optimal phase value from said CPU to said phase controller through said phase control data memory as phase control data, wherein said phase controller controls a phase delay amount for a clock pulse in accordance with the phase control data, supplies the phase-controlled clock pulse to an A/D converter as a sampling pulse, such that said A/D converter samples an analog video input signal at an optimal phase to convert the analog video input signal to a digital video signal, said digital video signal being supplied to a digital video signal processor, said digital video signal processor performing a color correction and a scaling processing on the digital video signal to convert the digital video signal to a digital video signal for display on a display unit, said display unit displaying the digital video signal as a video image.